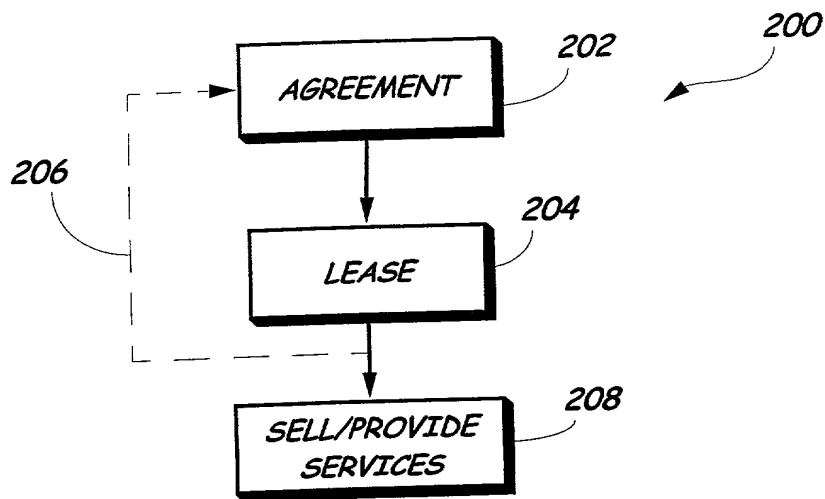
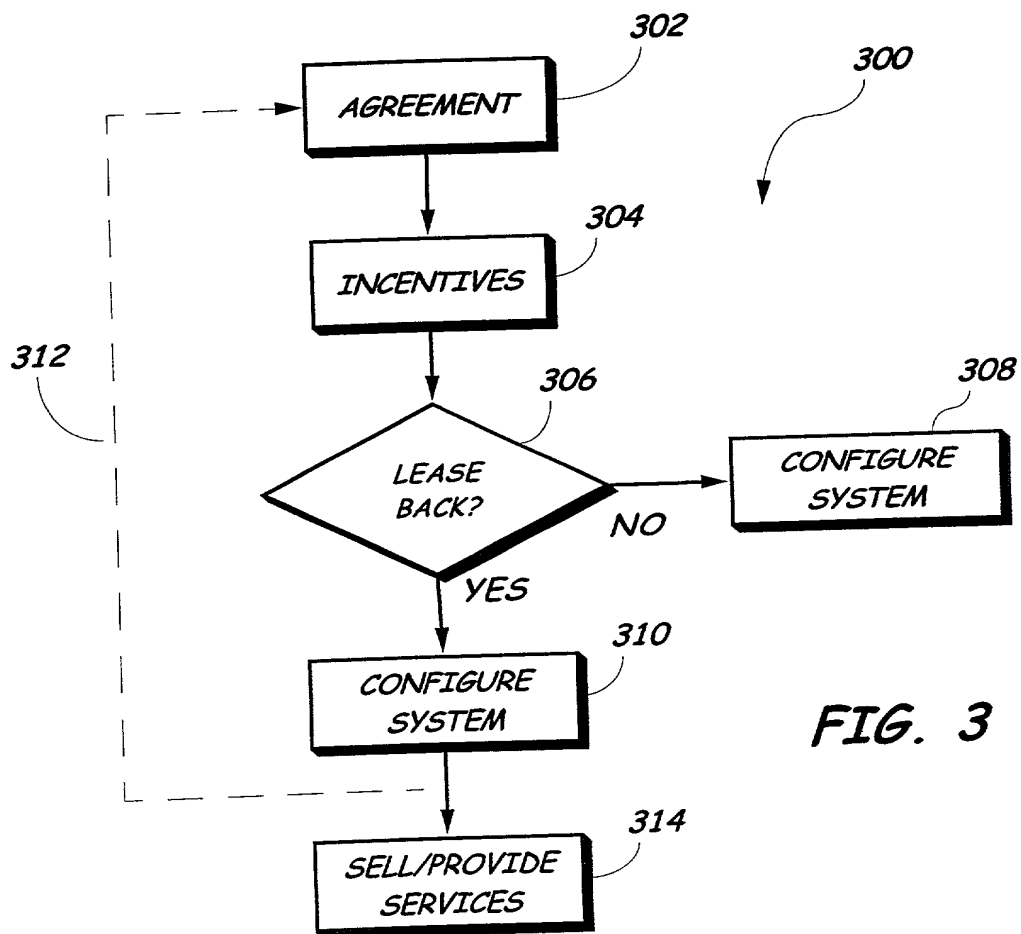


FIG. 1



**FIG. 2**



**FIG. 3**

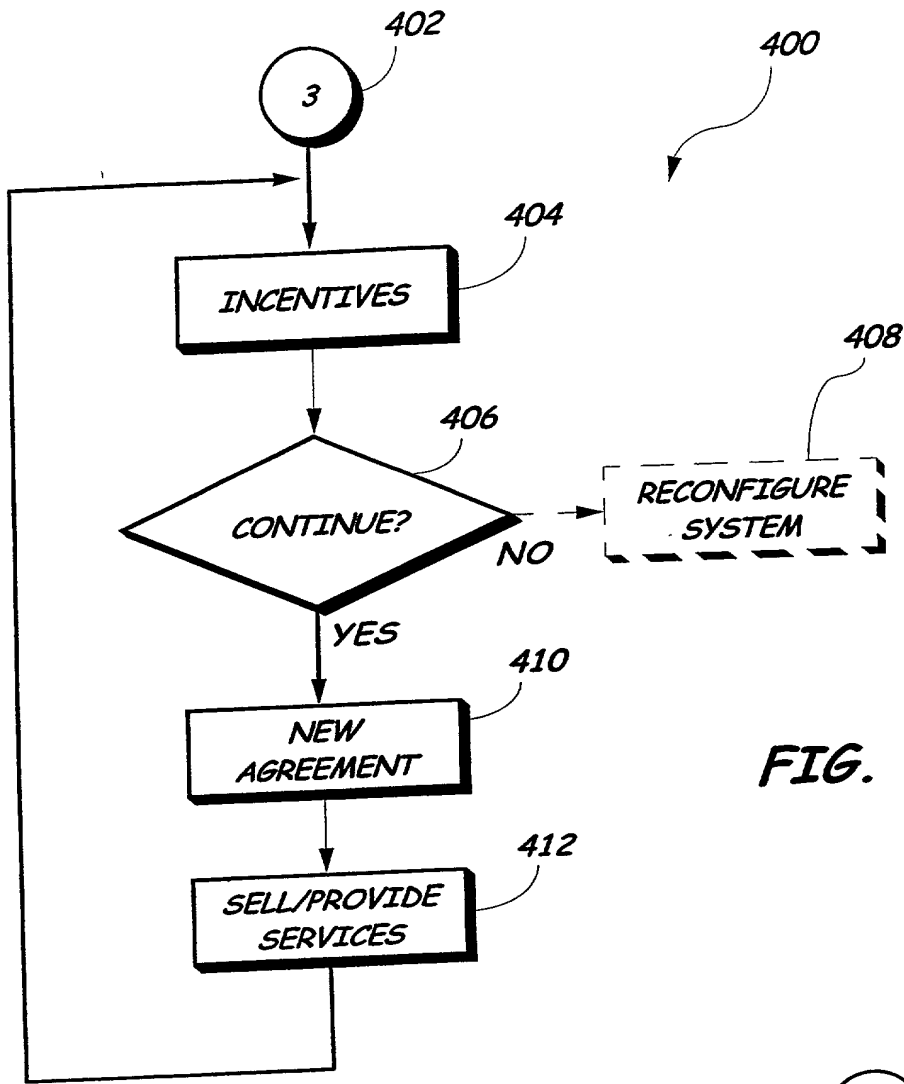


FIG. 4

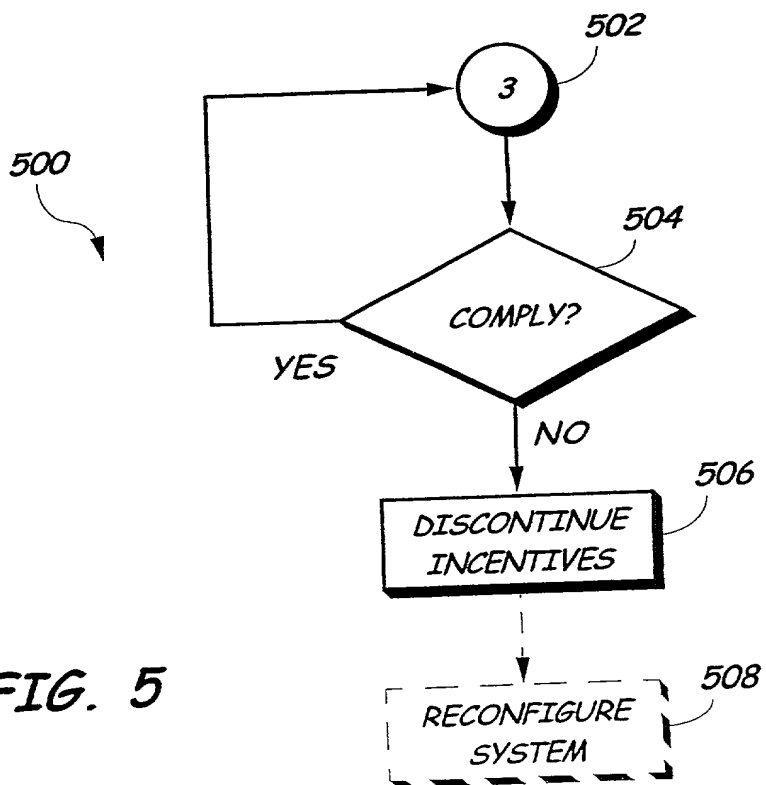


FIG. 5

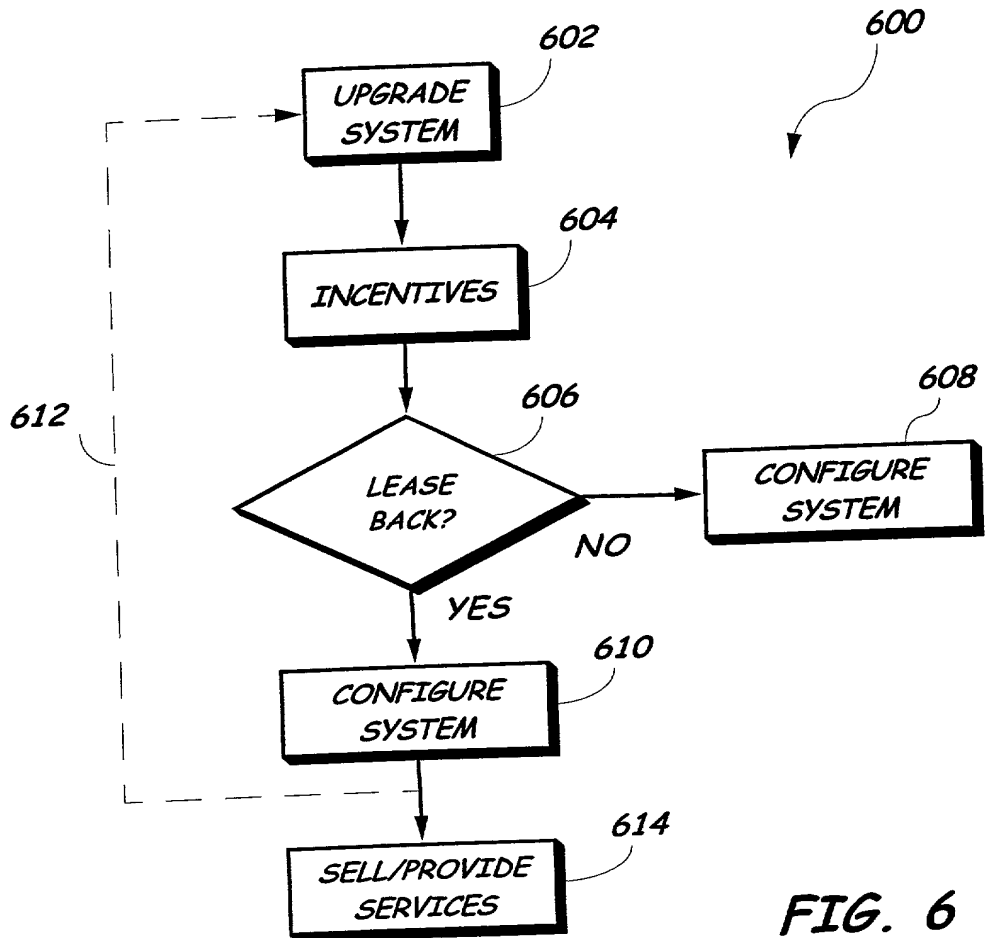


FIG. 6

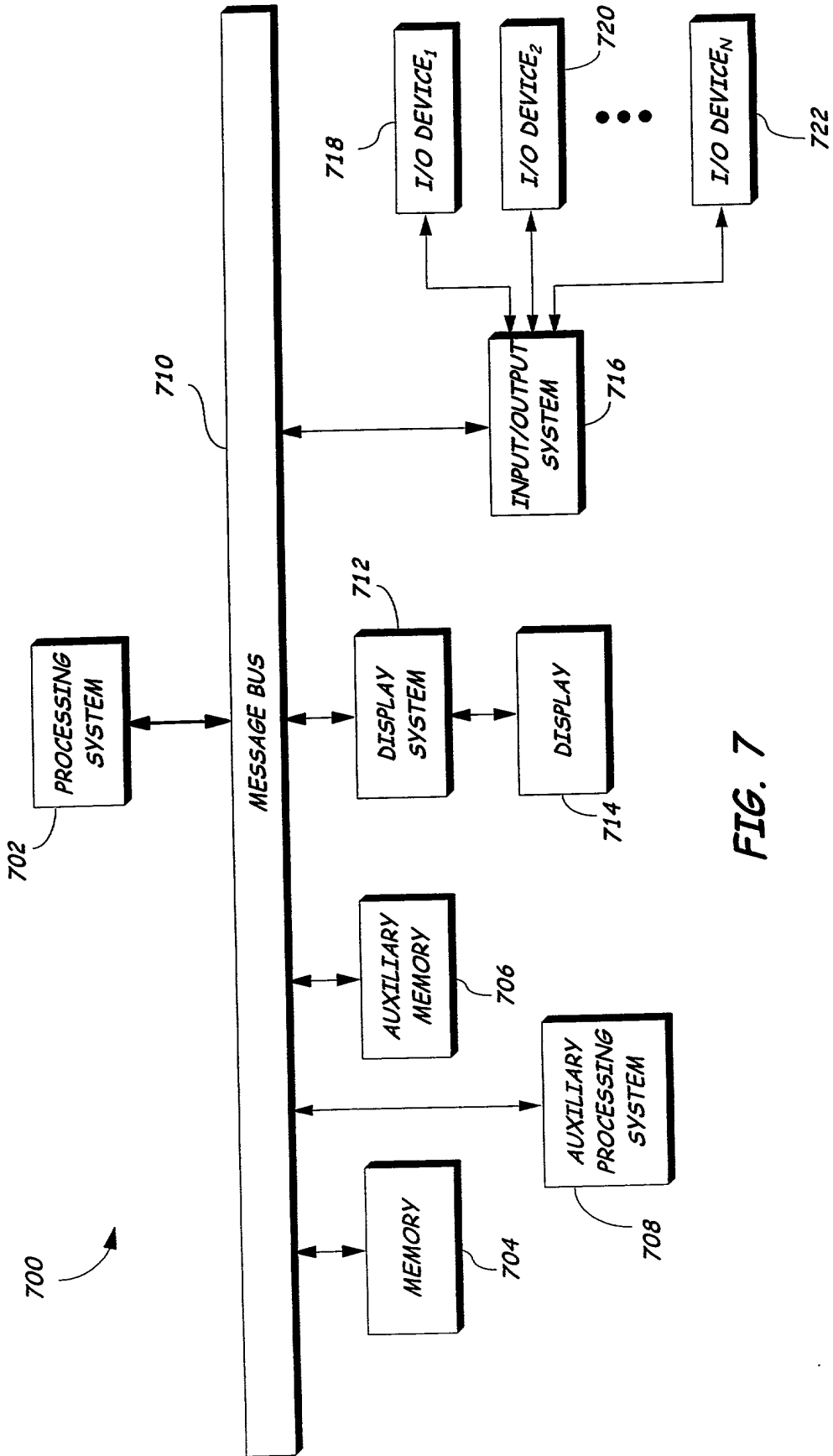


FIG. 7

FIG. 7 is a block diagram of a system architecture 700. The system architecture 700 includes a processing system 702, a memory 704, an auxiliary memory 706, an auxiliary processing system 708, a display system 712, a display 714, an input/output system 716, and a plurality of I/O devices 718, 720, 722. The processing system 702, the memory 704, the auxiliary memory 706, the auxiliary processing system 708, the display system 712, the display 714, the input/output system 716, and the I/O devices 718, 720, 722 are connected to a message bus 710.